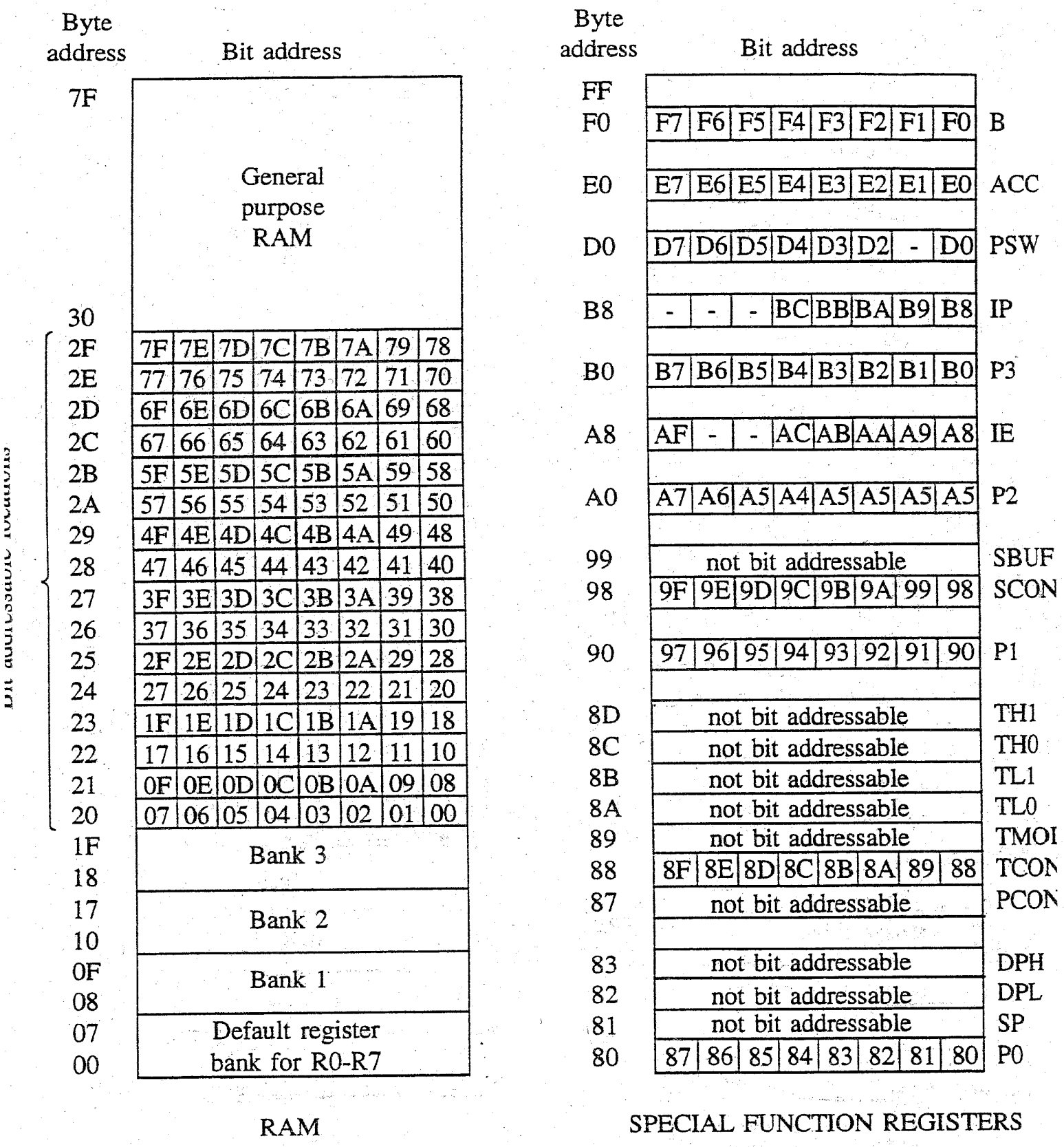
MNEMONIC		DESCRIPTION
Date Transfer Operations		
MOV	A,source	move source
MOV	A,#data	to destination
MOV	dest,A	
MOV	dest,source	
MOV	dest,#data	
MOV	DPTR,#data16	
MOVC	A,@A+DPTR	move from code
MOVC	A,@A+PC	memory
MOVX	A,@Ri	move from data
MOVX	A,@DPTR	memory
MOVX	@Ri,A	
MOVX	@DPTR,A	
PUSH	direct	push onto stack
POP	direct	pop from stack
XCH	A,source	exchange bytes
XCHD	A,@Ri	exchange low order digits
Boolean Variable Manipulation		
CLR	C	clear bit
CLR	bit	
SETB	C	set bit
SETB	bit	
CPL	C	complement bit
CPL	bit	
ANL	C,bit	AND bit with C
ANL	C,/bit	AND NOT bit with C
ORL	C,bit	OR bit with C
ORL	C,/bit	OR NOT bit with C
MOV	C,bit	move bit to bit
MOV	bit,C	
JC	rel	jump if C set
JNC	rel	if C not set
JB	bit,rel	jump if bit set
JNB	bit,rel	if bit not set
JBC	bit,rel	if set then clear
Program Branching		
ACALL	addr11	call subroutine
LCALL	addr16	
RET		return from sub.
RETI		from interrupt
AJMP	addr11	jump
LJMP	addr16	
SJMP	rel	
JMP	@A+DPTR	
JZ	rel	jump if A = 0
JNZ	rel	if A not = 0
CJNE	A,direct,rel	compare and jump
CJNE	A,#data,rel	if not equal
CJNE	Rn,#data,rel	
CJNE	@Ri,#data,rel	
DJNZ	Rn,rel	decrement and jump
DJNZ	direct,rel	if not zero
NOP		no operation

MNEMONIC		DESCRIPTION
Arithmetic Operations		
ADD	A,source	add source to A
ADD	A,#data	
ADDC	A,#source	add with carry
ADDC	A,#data	
SUBB	A,source	subtract from A
SUBB	A,#data	with borrow
INC	A	increment
INC	source	
DEC	A	decrement
DEC	source	
INC	DPTR	increment DPTR
MUL	AB	multiply A & B
DIV	AB	divide A by B
DA	A	decimal adjust A
Logical Operations		
ANL	A,source	logical AND
ANL	A,#data	
ANL	direct,A	
ANL	direct,#data	
ORL	A,source	logical OR
ORL	A,#data	
ORL	direct,A	
ORL	direct,#data	
XRL	A,source	logical XOR
XRL	A,#data	
XRL	direct,A	
XRL	direct,#data	
CLR	A	clear A
CPL	A	complement A
RL	A	rotate A left
RLC	A	(through C)
RR	A	rotate A right
RRC	A	(through C)
SWAP	A	swap nibbles

LEGEND

Rn	register addressing using R0–R7
direct	8-bit internal address (00H-FFH)
@Ri	indirect addressing using R0 or R1
source	any of [Rn,direct,@ri]
dest	any of [Rn,direct,@ri]
#data	8-bit constant included in instr.
#data 16	16-bit constant
bit	8-bit direct address of bit
rel	signed 8-bit offset
addr11	11-bit address in current 2k page
addr16	16-bit address


Byte address
Bit address
7F
General purpose RAM
30
2F 7F 7E 7D 7C 7B 7A 79 78
2E 77 76 75 74 73 72 71 70
2D 6F 6E 6D 6C 6B 6A 69 68
2C 67 66 65 64 63 62 61 60
2B 5F 5E 5D 5C 5B 5A 59 58
2A 57 56 55 54 53 52 51 50
29 4F 4E 4D 4C 4B 4A 49 48
28 47 46 45 44 43 42 41 40
27 3F 3E 3D 3C 3B 3A 39 38
26 37 36 35 34 33 32 31 30
25 2F 2E 2D 2C 2B 2A 29 28
24 27 26 25 24 23 22 21 20
23 1F 1E 1D 1C 1B 1A 19 18
22 17 16 15 14 13 12 11 10
21 0F 0E 0D 0C 0B 0A 09 08
20 07 06 05 04 03 02 01 00
1F
18
Bank 3
17
10
Bank 2
0F
08
Bank 1
07
00
Default register bank for R0-R7
Bit addressable locations
RAM
Byte address
Bit address
FF
F0 F7 F6 F5 F4 F3 F2 F1 F0 B
E0 E7 E6 E5 E4 E3 E2 E1 E0 ACC
D0 D7 D6 D5 D4 D3 D2 - D0 PSW
B8 - - - BC BB BA B9 B8 IP
B0 B7 B6 B5 B4 B3 B2 B1 B0 P3
A8 AF - - AC AB AA A9 A8 IE
A0 A7 A6 A5 A4 A5 A5 A5 A5 P2
99 not bit addressable SBUF
98 9F 9E 9D 9C 9B 9A 99 98 SCON
90 97 96 95 94 93 92 91 90 P1
8D not bit addressable TH1
8C not bit addressable TH0
8B not bit addressable TL1
8A not bit addressable TL0
89 not bit addressable TMOI
88 8F 8E 8D 8C 8B 8A 89 88 TCON
87 not bit addressable PCON
83 not bit addressable DPH
82 not bit addressable DPL
81 not bit addressable SP
80 87 86 85 84 83 82 81 80 P0
SPECIAL FUNCTION REGISTERS